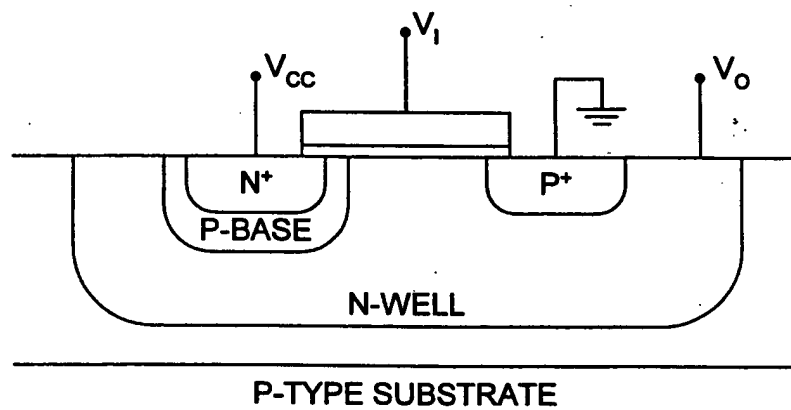
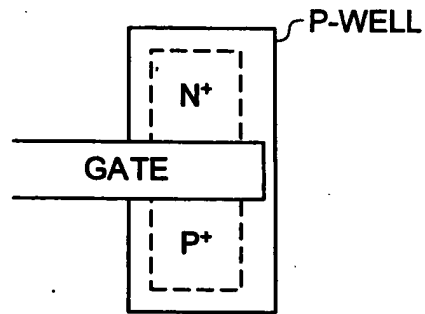
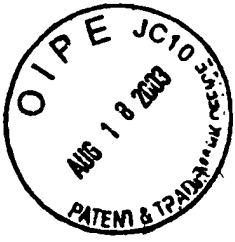


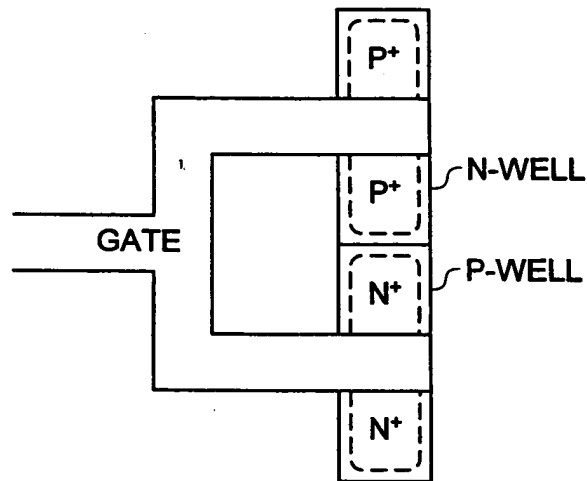
**FIGURE 1**



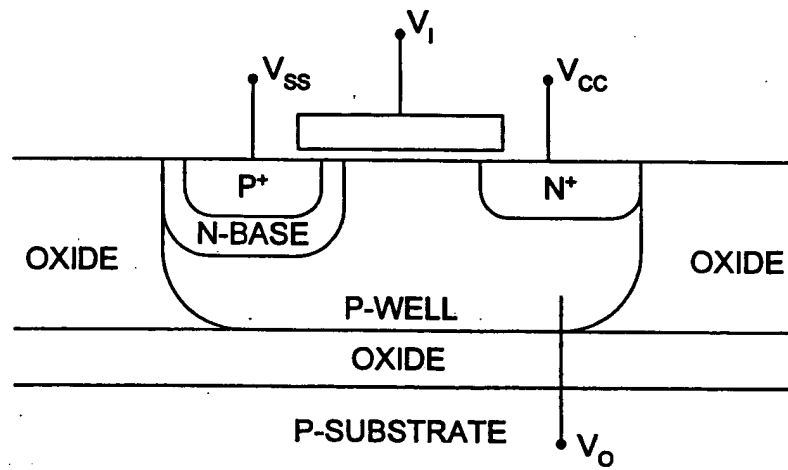
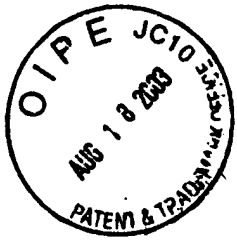
**FIGURE 2**



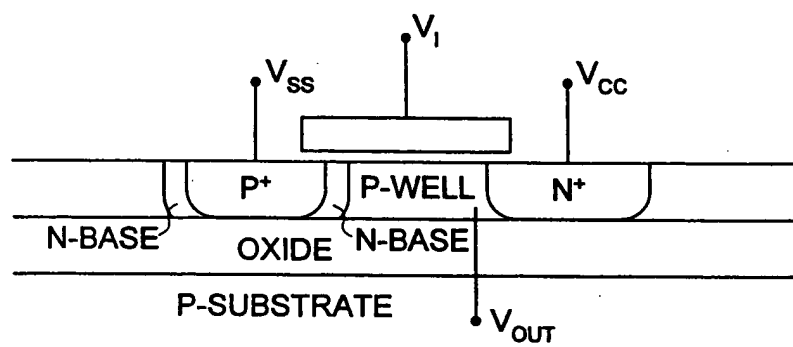
**FIGURE 3**



**FIGURE 4**  
(PRIOR ART)



**FIGURE 5**



**FIGURE 6**

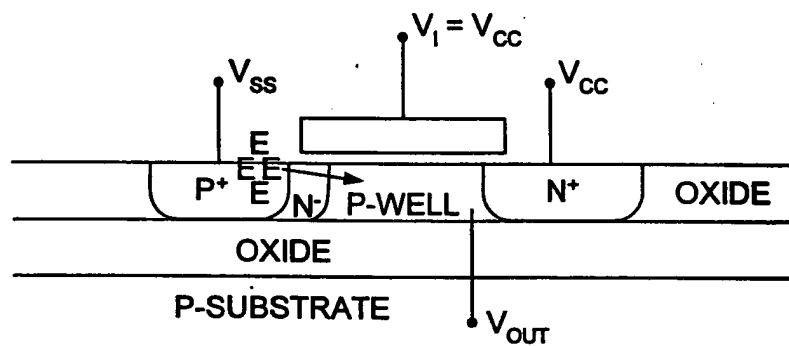
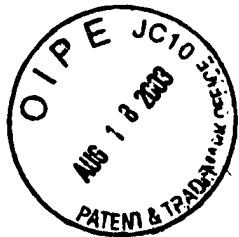


FIGURE 7

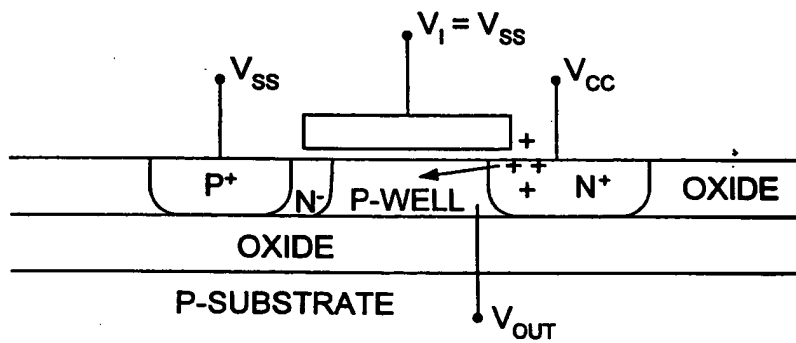
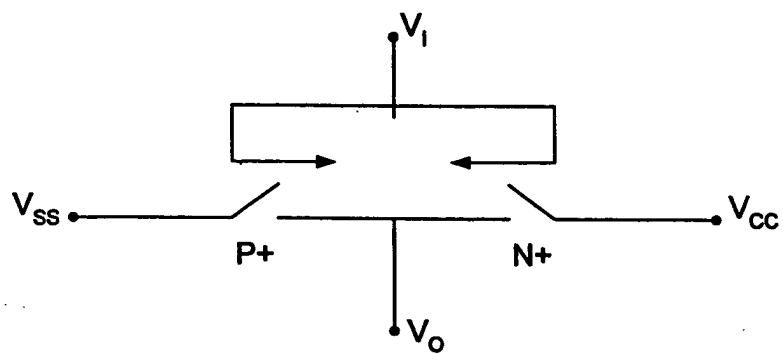
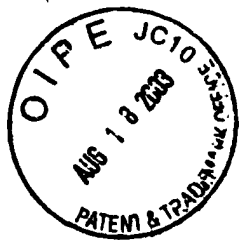
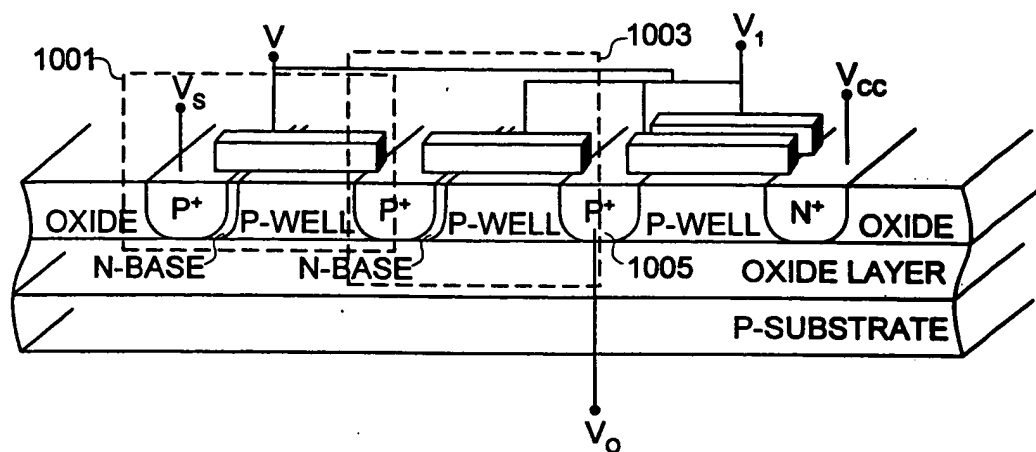


FIGURE 8

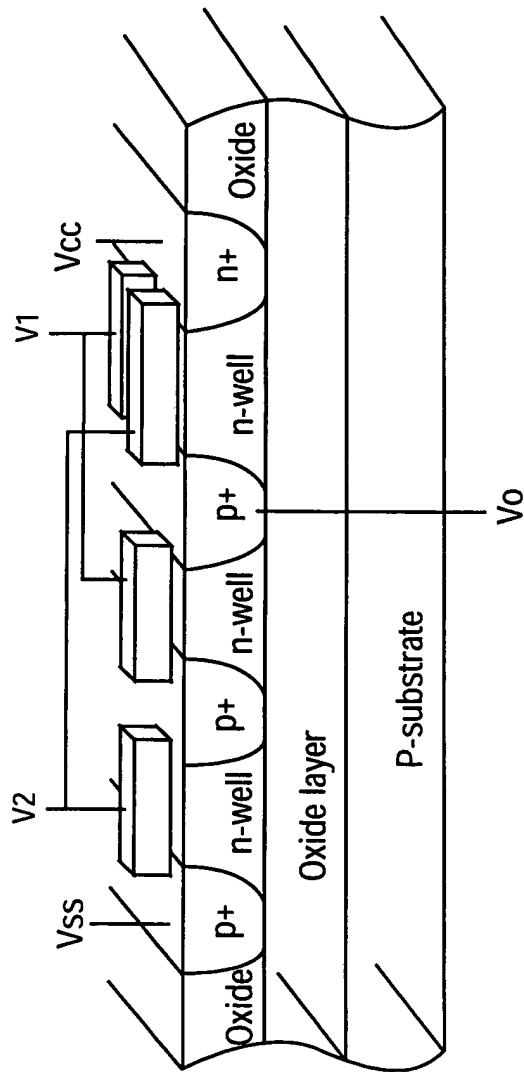
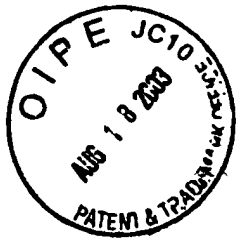


**FIGURE 9**

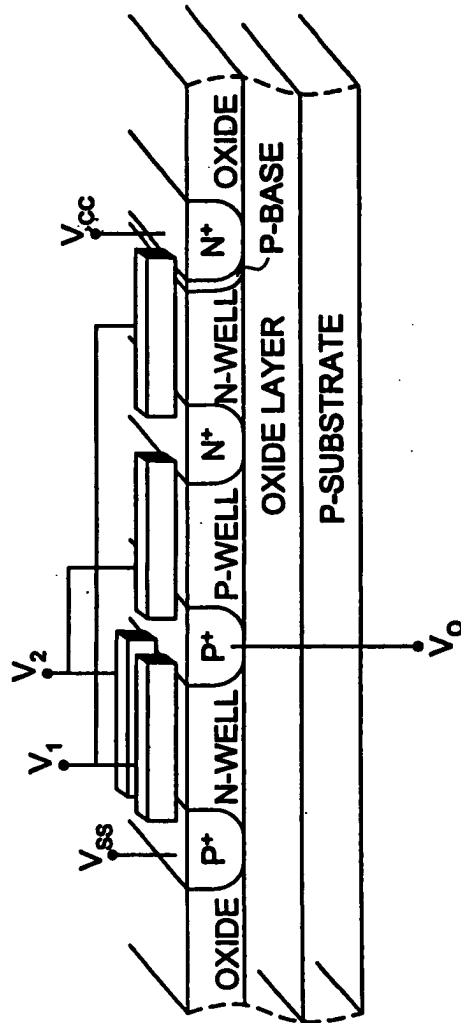
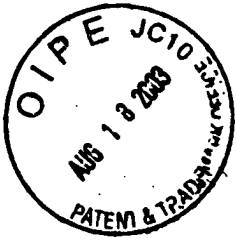


A cross-sectional diagram of a 1T1R device structure. The structure consists of a P-SUBSTRATE at the base, followed by an N-BASE layer, and an OXIDE LAYER on top. The OXIDE LAYER contains several regions: P+, P-WELL, P+, P-WELL, N+, P-WELL, N+, and OXIDE. A gate stack is formed on top of the OXIDE LAYER, consisting of a gate oxide layer (1103) and a gate electrode (1101). The gate electrode is divided into two sections: a left section (1105) and a right section (1101). The left section (1105) is connected to a voltage source  $V_s$ . The right section (1101) is connected to a voltage source  $V_c$ . The gate oxide layer (1103) is connected to a voltage source  $V_1$ . The P+ regions are connected to a common voltage source  $V_0$ .

## FIGURE 11

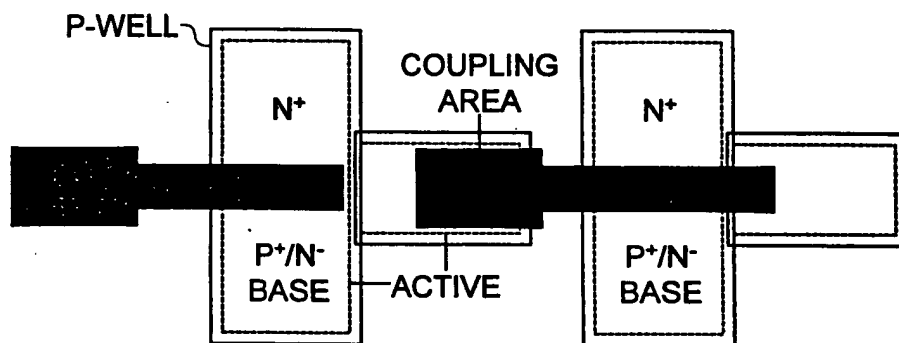
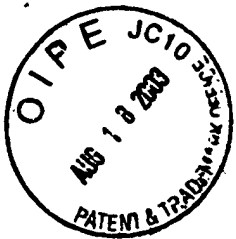


**FIG. 10A**



# FIGURE 11A





**FIGURE 12**